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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/085,755	05/27/1998	FRAMPTON ERROLL ELLIS, III	GNC12US	7351

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EXAMINER	
STRANGE, AARON N	
ART UNIT	**PAPER NUMBER**
2153	

MAIL DATE	DELIVERY MODE
12/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/085,755	ELLIS, III, FRAMPTON ERROLL	
	Examiner	Art Unit	
	Aaron Strange	2153	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9,10,12-18,20,22,25-27,30-42,53,55-57,61-64 and 66-103* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9,10,12-18,20,22,25-27,30-42,53,55-57,61-64 and 66-103* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The Examiner would like to note that the present application has been reassigned to a new Examiner.

Double Patenting

2. Applicant has failed to traverse the double patenting rejections of claims 9, 10, 12-18, 20, 22, 25-27, 30-42, 53, 55-57, 61-64 and 66-97, presented in the Office action of 7/10/07. Therefore, those rejections are maintained.

A timely filed terminal disclaimer in compliance with 37 CFR 1.321 (c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 35 CFR 1.130(b).

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b). Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 9-10, 12-18, 20, 22, 25-27, 30-42, 53, 55-57, 61-64, and 66-97 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over the claims U.S. Patent Number 7,047,275 and Slater, "The Microprocessor Today" and Steinert-Threlkeld, "NEW BREED OF CHIP TI develops a super circuit" and Applicant's admitted prior art.

Although the conflicting claims are not identical, they are not patentably distinct from each other. Refer to the tables and remarks below for specific claim mappings and further explanation.

5. Claims 9-10, 12-18, 20, 22, 25-27, 30-42, 53, 55-57, 61-64, and 66-97 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over the claims U.S. Patent Number 7,035,906.

Although the conflicting claims are not identical, they are not patentably distinct from each other. Refer to the tables and remarks below for specific claim mappings and further explanation.

6. Claims 9-10, 12-18, 20, 22, 25-27, 30-42, 53, 55-57, 61-64, and 66-97 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over the claims U.S. Patent Number 6,167,428 and Slater, "The Microprocessor Today" and Steinert-Threlkeld, "NEW BREED OF CHIP TI develops a super circuit" and Applicant's admitted prior art.

Although the conflicting claims are not identical, they are not patentably distinct from each other. Refer to the tables and remarks below for specific claim mappings and further explanation.

7. Claims 9-10, 12-18, 20, 22, 25-27, 30-42, 53, 55-57, 61-64, and 66-97 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 35-49 of copending Application No. 09/935,779 and Slater, "The Microprocessor Today" and Steinert-Threlkeld, "NEW BREED OF CHIP TI develops a super circuit" and Applicant's admitted prior art.

Although the conflicting claims are not identical, they are not patentably distinct from each other. Refer to the tables and remarks below for specific claim mappings and further explanation. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

U.S. Patent Number # 7,047,275	Instant Application # 09/085,755
1. An apparatus, comprising: a firewall configured to operate in a personal computer, which is configured to operate with other computers connected in a network;	9. A system, comprising: at least one personal computer, said personal computer configured to operate with a t least one other computer connected to a network;
Said personal computer including at least two microprocessors (note some power management component is required for the processor to be able to operate);	Said personal computer including at least two processing units, and said microchip including at least one power management component;
Said firewall configured to both allow and deny access to at least a first microprocessor of said personal computer by at least one of said other computers of said network during a shared operation involving said personal computer and said at least one of said other computers of said network.	Said personal computer including at least one internal firewall, said internal firewall capable of allowing and/or denying access to portions of said microchip both to at least one user of said personal computer and to at least one user of said microchip from said network during shared use of said microchip.

The '275 claims include two processors within the personal computer however the '275 claims failed to disclose means for at least one user of said personal computer

to control both processing units. Nonetheless it would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to allow the user of a personal computer system to control all the resources of his or her system, so that the user can take full advantage of his or her system by utilizing all available resources within the system.

The '275 claims failed to specifically recite the two processors are including within a single microchip. Slater discusses the state of the art of microprocessor design in 1996. Slater discloses reducing system cost by integrating more functions on a chip and microprocessors are evolving toward system on a chip. Slater teaches all the components of a PC onto the same chip as the microprocessor. (See pages 42-43). Furthermore this concept of system-on-a-chip and its benefits were widely known well before 1996, dating back to at least 1992, see Steinert-Threlkeld, "NEW BREED OF CHIP TI develops a super circuit" pages 1-2 and in particular pg 2 ¶s 3-5, "TI will be trying to squeeze onto a single chip most if not all of the contents of the main printed circuit board in a personal computer." Also Applicant himself admits that the concept of placing all the components of a PC onto a single chip was widely known in the art at the time of Applicant's invention (See Applicant's CIP parent patent 6,732,141, Col 15, lines 34-43). Hence, it would have been obvious for one of ordinary skill in the art at the time of the invention to put all components of a PC onto a single microchip, including the two microprocessors found in the personal computer of the '275 claims, because it would have provided a PC that results in more speed, less weight, and less power consumption in a smaller space (see inter alia, Steinert-Threlkeld pg 2, ¶ 4).

U.S. Patent Number # 7,035,906	Instant Application # 09/085,755
1. A microchip for a personal computer comprising: a microprocessor with a control unit and at least two processing unit, the control unit including allowing a user of the personal computer to control the processing units; (note some power management component is required for the processing units to be able to operate);	9. A system, comprising: at least one personal computer, said personal computer configured to operate with a t least one other computer connected to a network; Said personal computer including at least two processing units, said control unit including means for a at least one user of said personal computer to control said at least two processing units, and said microchip including at least one power management component;
A firewall configured to permit access through the network to a processing unit to execute all or a portion of a shared computer processing operation involving the personal computer and another personal computer.	Said personal computer including at least one internal firewall, said internal firewall capable of allowing and/or denying access to portions of said microchip both to at least one user of said personal computer and to at least one user of said microchip from said network during shared use of said microchip.

The rejections over U.S. Patent Number 6,167,428 and application number 09/935,779 are based on a similar rationale as applied above.

Claim Rejections - 35 USC § 112

8. Claims 9, 10, 12-18, 20, 22, 25-27, 30-42, 53, 55-57, 61-64 and 66-103 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. The claims are generally indefinite and are replete with typographical and grammatical errors. Several examples have been provided below, but these should not be considered comprehensive. Applicant is required to correct all of the issues identified below as well as any remaining.

10. The limitation "wherein said network includes a World Wide Web", in claim 18, is unclear. It is unclear if this is intended to refer to the well-known World Wide Web. If so, the claim should be amended to recite "the World Wide Web".

11. The limitation "wherein said personal computer includes at least one direct wireless connection", in claim 22, is unclear. It is unclear how a computer may "include" a connection.

12. The limitation "system of claim 9, further comprising a shared processing operation", in claim 27, is unclear. It is unclear how a system may "comprise" an operation.

13. Claim 34 depends from cancelled claim 11.

14. Claim 38 recites the limitation "said other computers" in line 3. There is insufficient antecedent basis for this limitation in the claim. At least claim 39 also contains this limitation.

15. As noted above, these examples are not intended to be an exhaustive list. Numerous claims, similar in scope to those identified above, contain similar limitations. All claims should be reviewed, with particular emphasis placed on ensuring proper dependency and antecedent basis for all claim limitations. If there are any questions, Applicant is invited to contact the Examiner to schedule an interview.

Allowable Subject Matter

16. Claims 9, 10, 12-18, 20, 22, 25-27, 30-42, 53, 55-57, 61-64 and 66-103 appear to be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron Strange whose telephone number is 571-272-3959. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glen Burgess can be reached on 571-272-3949. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AS
11/30/07

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